IN THE SPECIFICATION:

Please amend the paragraph beginning at line 6, page 2 as follows:

Fig. 8 is a cross sectional view showing an example of the structure of a compound semiconductor device having multi-level wiring layers. A semiconductor substrate 100 has [the] a structure [that] in which a functional semiconductor region is formed on an underlying substrate of GaAs or InP. A low resistance layer is formed in the upper surface layer of the semiconductor substrate 100, and a source electrode 101 and a drain electrode 102 are formed on the low resistance layer in ohmic contact therewith. The surface low resistance layer is removed in the intermediate area between the source electrode 101 and drain electrode 102 to form a recess area. On this recess area, a mushroom gate 105 is formed.

Please amend the paragraph beginning at line 16, page 2 as follows:

The mushroom gate 105 has a stem (hereinafter called a fine gate) which contacts the semiconductor substrate 100 and is narrow along the current direction and a head (hereinafter called an over gate) which is broad along the current direction. In order to enhance [a] high speed operation the size of the fine gate along the current direction is made narrow, and in order to reduce the gate resistance the size of the over gate along the current direction is made broad.

Please amend the paragraph beginning at line 7, page 10 as follows:

Fig. 1G shows the cross sectional structure near the gate electrode G with the filler layer being removed at least from the active region. The gate electrode G is surrounded with the hollow

space H. The interface between the hollow space H and interlayer insulating film IL is a curved surface. The interlayer insulating film IL does not contact the main portion of the gate electrode G. Since the dielectric constant of the hollow space H is 1, an increase in the parasitic capacitance of the gate electrode G can be greatly suppressed ~~greatly~~.